

Unit I

1. Define Threshold voltage

The threshold voltage V_T for a MOS transistor can be defined as the voltage between the gate and the source terminals below which the drain to source current effectively drops to zero.

Define body effect or substrate bias effect.

The threshold voltage V_T is not a constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This effect is called the body effect or substrate bias effect.

2. Give the different modes of operation of MOS transistor

Cut off mode

Linear mode

Saturation mode

3. What are the different regions of operation of a MOS transistor?

a. Cut off region

Here the current flow is essentially zero (accumulation mode)

b. Linear region

It is also called weak inversion region where the drain current is dependent on the gate and the drain voltage w. r. to the substrate.

c. Saturation region

Channel is strongly inverted and the drain current flow is ideally independent of the drain-source voltage (strong-inversion region).

4. Give the expressions for drain current for different modes of operation of MOS transistor.

a. Cut off region

$$I_D = 0$$

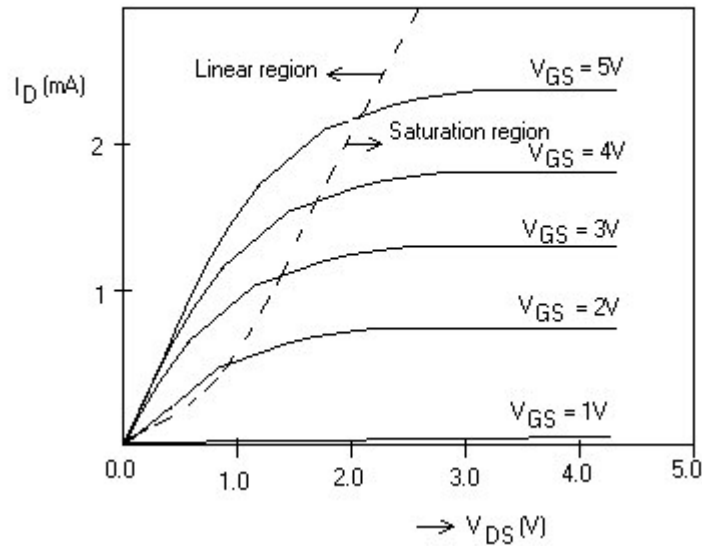
b. Linear region

$$I_D = k_n [(V_{GS} - V_T) V_{DS} - V_{DS}^2/2]$$

c. Saturation region

$$I_D = (k_n/2) (V_{GS} - V_T)^2$$

5. Plot the current-voltage characteristics of a nMOS transistor.



6. Define accumulation mode.

The initial distribution of mobile positive holes in a p type silicon substrate of a mos transistor for a voltage much less than the threshold voltage

7. What are the secondary effects of MOS transistor?

- a. Threshold voltage variations
- b. Source to drain resistance
- c. Variation in I-V characteristics
- d. Subthreshold conduction
- e. CMOS latchup

8. What is CMOS latchup? How it can be prevented?

The MOS technology contains a number of intrinsic bipolar transistors. These are especially troublesome in CMOS processes, where the combination of wells and substrates results in the formation of p-n-p-n structures. Triggering these thyristor like devices leads to a shorting of V_{DD} & V_{SS} lines, usually resulting in a destruction of the chip.

The remedies for the latch-up problem include:

- (i) an increase in substrate doping levels with a consequent drop in the value of

R_{psubs} .

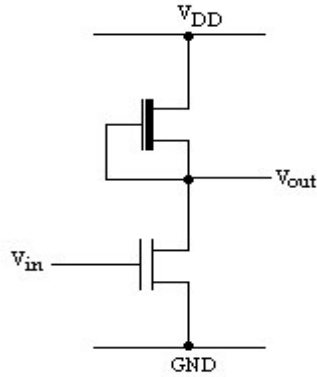
- (ii) reducing R_{nwell} by control of fabrication parameters and ensuring a low contact resistance to V_{DD} .
- (iii) by introducing guard rings.

9. What are the different fabrication processes available to CMOS technology?

- a. p-well process
- b. n-well process
- c. Twin-tub process
- d. Silicon On Insulator (SOI) / Silicon On Sapphire (SOS) process

Unit II

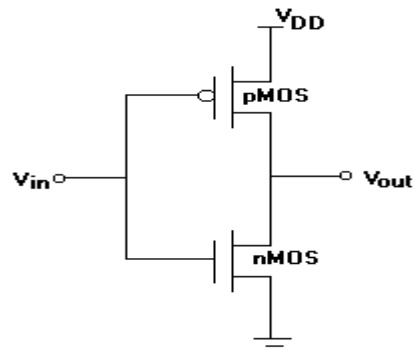
1. Draw the circuit of a nMOS inverter.



2. Give the expression for pull-up to pull-down ratio ($\frac{Z_{pu}}{Z_{pd}}$) for an nMOS inverter driven by another nMOS inverter.

$$V_{inv} = V_T - \frac{V_{Td}}{\sqrt{\frac{Z_{p,u}}{Z_{p,d}}}}$$

3. Draw the circuit of a CMOS inverter.



4. What are the advantages of CMOS inverter over the other inverter configurations?

- a. The steady state power dissipation of the CMOS inverter circuit is negligible.
- b. The voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0V and V_{DD} . This results in high noise margin.

5. What are stick diagrams?

Stick diagrams are used to convey layer information through the use of a color code. A stick diagram is a cartoon of a chip layout. They are not exact models of layout. The stick diagram represents the rectangles with lines which represent wires and component symbols.

6. What are the different color codes used for single poly silicon nMOS technology?

n-diffusion (n-diff.) and other thinoxide regions	-green
Polysilicon (poly.)	- red
Metal 1 (metal)	- blue
Implant	- yellow
Contacts	- black or brown (buried)

7. What are design rules?

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. Design rules are used to produce workable mask layouts from which the various layers in silicon will be formed or patterned.

8. What are Lambda (λ) - based design rules?

These rules popularized by Mead and Conway are based on a single parameter, λ , which characterizes the linear feature – the resolution of the complete wafer implementation process – and permits first order scaling. They have been widely used, particularly in the educational context and in the design of multiproject chips. In lambda based design rules, all paths in all layers will be dimensioned in λ units and subsequently λ can be allocated an appropriate value compatible with the feature size of the fabrication process. Design rules, specify line widths, separations, and extensions in terms of λ

9. Define a superbuffer.

A superbuffer is a symmetric inverting or noninverting gate that can supply or remove large currents and switch large capacitive loads faster than a standard inverter.

What are BiCMOS Gates?

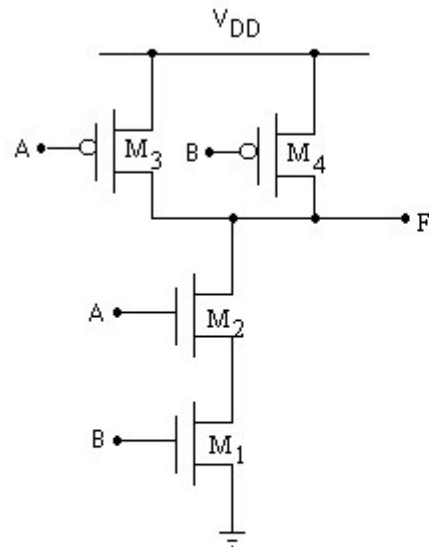
When bipolar and MOS technology are merged, the resulting circuits are referred to as biCMOS circuits. High gain vertical npn transistors with their collectors tied to the positive rail, and medium-gain lateral npn transistors are both compatible with conventional CMOS processing. BiCMOS gates can be used to improve the performance of line drivers and sense amplifiers.

Unit III

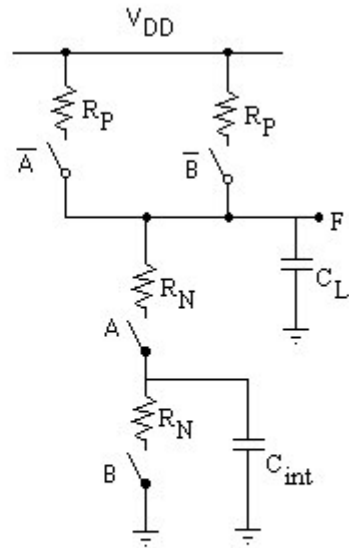
1. What are the static properties of complementary CMOS Gates?

- a. They exhibit rails-to-rail swing with $V_{OH} = V_{DD}$ and $V_{OL} = GND$.
- b. The circuits have no static power dissipation, since the circuits are designed such that the pull-down and pull-up networks are mutually exclusive.
- c. The analysis of the DC voltage transfer characteristics and the noise margins is more complicated than for the inverter, as these parameters depend upon the data input patterns applied to the gate.

2. Draw the equivalent RC model for a two-input NAND gate.



(a) Two - input NAND



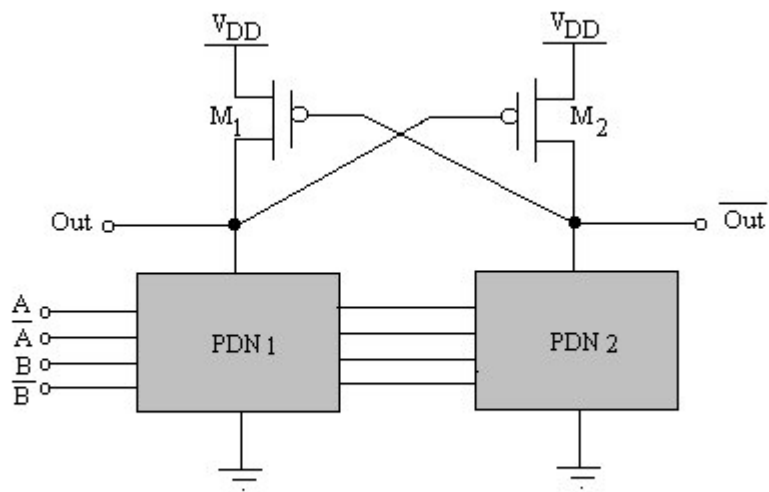
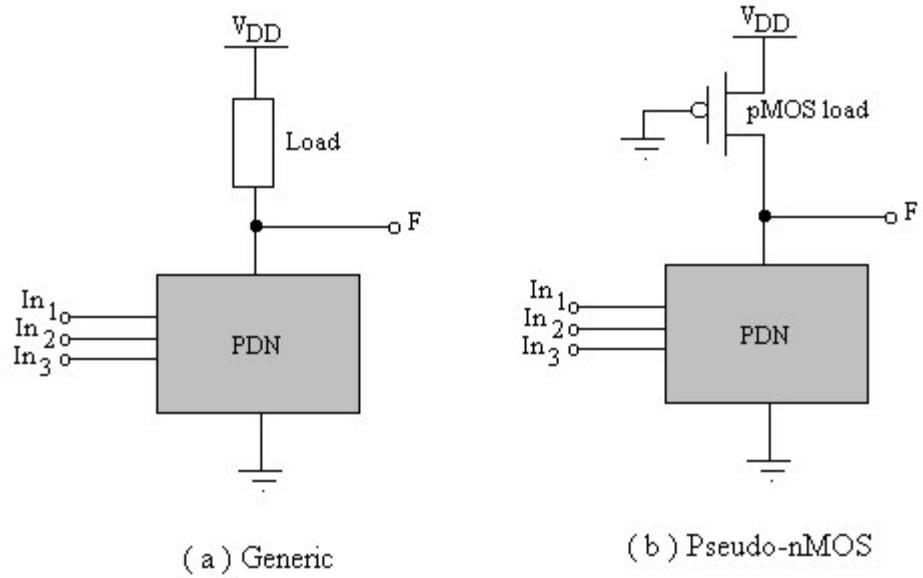
(b) RC equivalent circuit

3. What are the major limitations associated with complementary CMOS gate?

- a. The number of transistors required to implement an N fan-in gate is $2N$. This can result in a significantly large implementation area.
- b. The propagation delay of a complementary CMOS gate deteriorates rapidly as a function of the fan-in.

4. What is meant by ratioed logic?

In ratioed logic, a gate consists of an nMOS pull-down network that realizes the logic function and a simple load device, which replace the entire pull-up network. A ratioed logic which uses a grounded pMOS load is referred to as a pseudo-nMOS gate



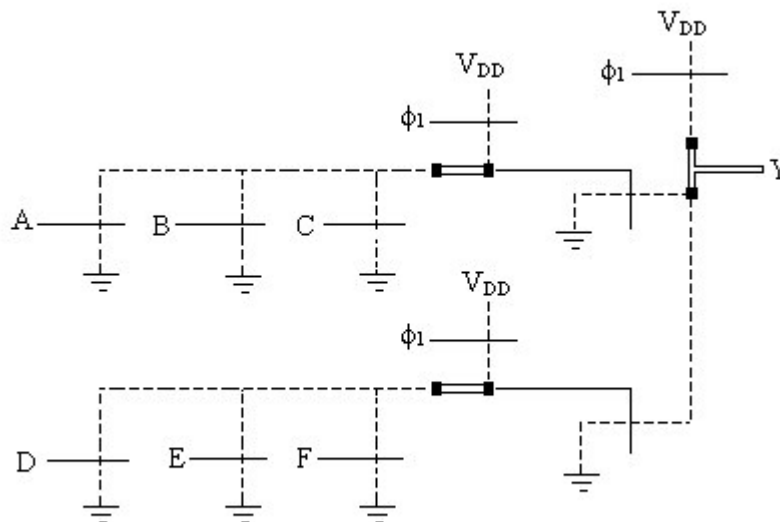
5. What is true single phase clocked register?

The True single-phase clocked register (TSPCR) uses a single clock, CLK. For the positive latch, when CLK is high, the latch is in the transparent mode and corresponds to two cascaded inverters; the latch is non-inverting, and propagates the input to the output. On the other hand, when CLK=0, both inverters are disabled, and the latch is in the hold mode.

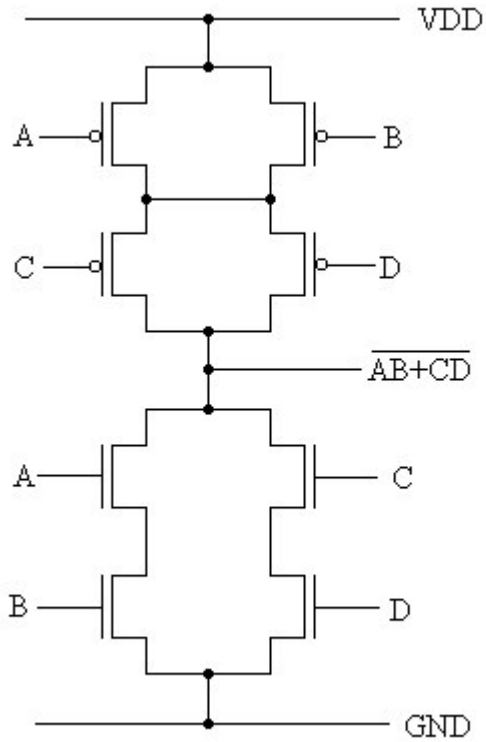
6. Define a tally circuit.

A tally circuit counts the number of inputs that are high and outputs the answer. If there are N inputs there are N + 1 possible outputs, corresponding to 0, 1, 2, N inputs that are high.

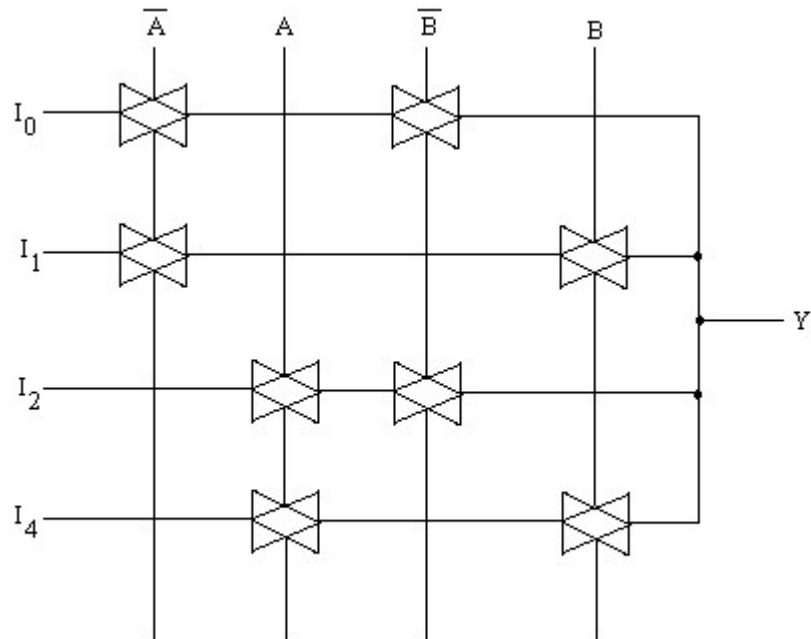
7. Give the NAND-NAND implementation of $\gamma = ABC + DEF$ in stick form.



8. Draw the Static AOI CMOS gates to realize $\gamma = (AB + CD)$.

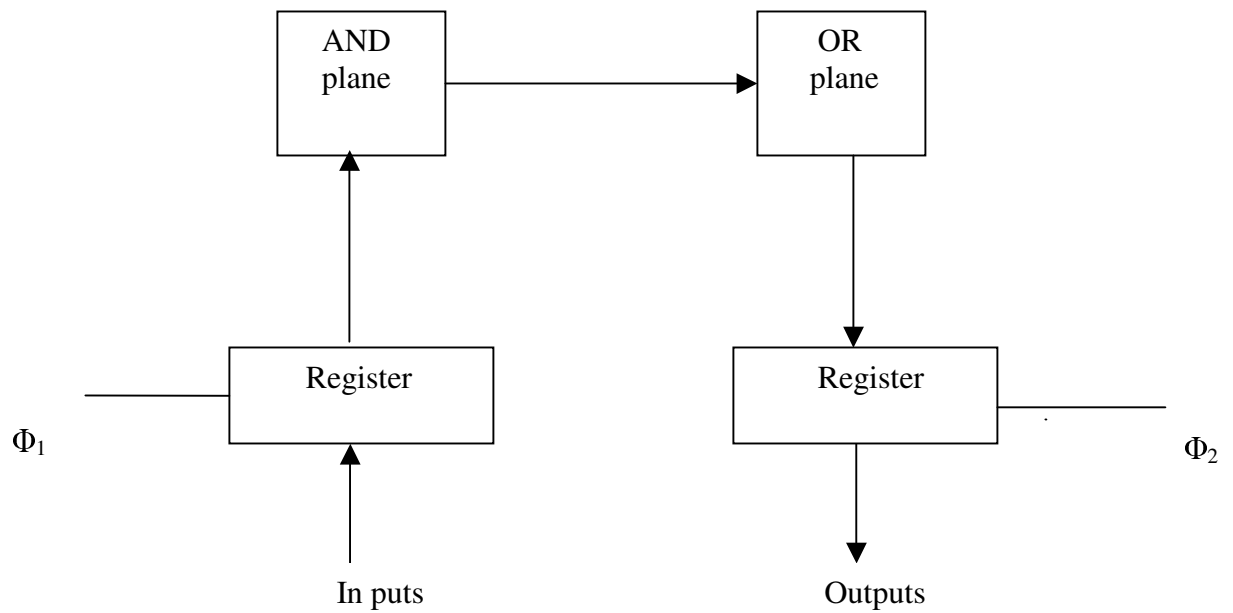


9. Draw the CMOS implementation of 4-to-1 MUX using transmission gates .



Unit IV

1. Give the basic nMOS PLA structure.



The basic PLA structure consists of an AND plane driving an OR plane. The terminology corresponds to a sum of products (SOP) realization of the desired function. The SOP realization converts directly into a NAND-NAND implementation. When a product of sums (POS) realization is desired, it can be implemented in OR-AND or NOR-NOR logic. In either case, the first array is referred to as the AND plane, and the second array as the OR plane. The line connecting the AND plane to the OR plane are called the product lines.

2. What do you mean by CMOS PLA.

The basic CMOS PLA is obtained by providing a well and replacing the pull-up devices in the NAND-NAND array or in the NOR-NOR array with enhancement mode pMOS devices. The CMOS array can be precharged or not, and can be clocked

with the same two-phase clocking scheme as used for the MOS PLA. CMOS PLA design offers many more varieties of layout than does nMOS.

3. Define finite state machine.

When feedback is added to the AND OR PLA structure, the PLA becomes a finite state machine (FSM). An FSM can be designed as a Mealy Machine or a Moore Machine. The Mealy machine has outputs, which may change with input changes in an asynchronous manner and cause erroneous behavior. Hence, the Mealy machine should be avoided whenever possible. The Moore machine has outputs which depend upon and change only with state changes, since all the outputs of the Boolean-logic block go through a state register, and are synchronously clocked.

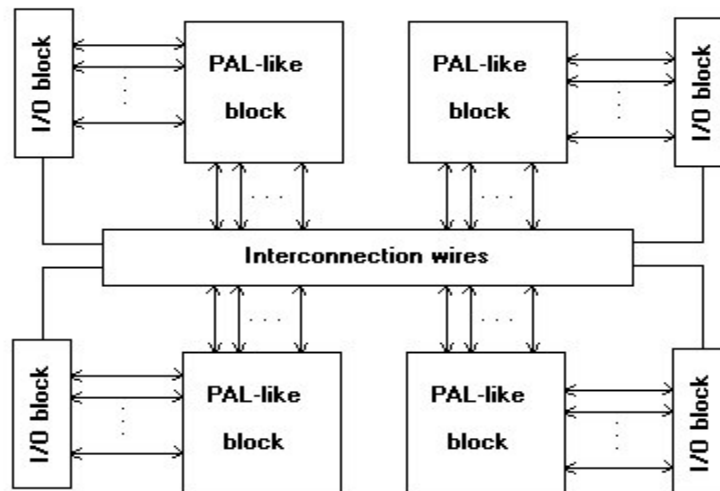
4. What are the importance of the PLA/FSM in VLSI?

- (i) Regularity : It has a standard, easily expandable layout.
- (ii) Convenience : Little design effort is required.
- (iii) Compacted : It is efficient for small circuits.
- (iv) Modularity : It makes it possible to design hierarchical PLAs and FSMs into

large sequential systems.

- (v) Suitability to being computer generated.

5. Give the structure of a CPLD.

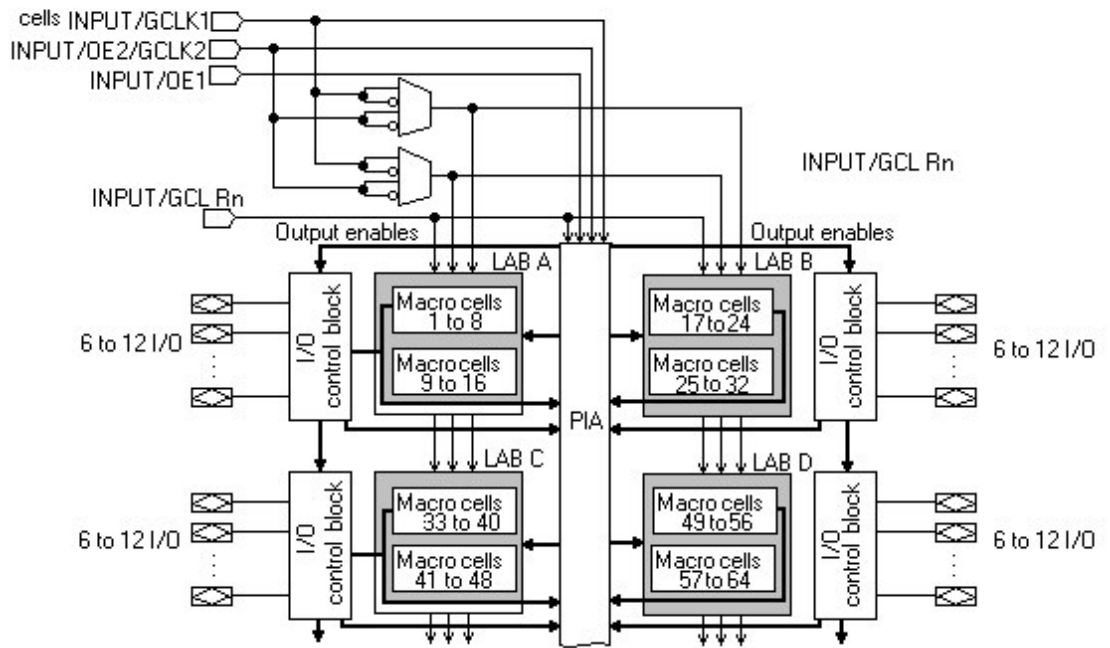


A CPLD comprises multiple circuit blocks on a single chip, with internal wiring resources to connect the circuit blocks. Each circuit block is similar to a PLA or a PAL. It includes four PAL like blocks that are connected to a set of interconnection wires. Each PAL like block is also connected to a sub circuit labeled I/O block, which is attached to a number of the chip's input and output pins.

6. Give the CPLD packages available.

- a. **PLCC package:** The PLCC package has pins that “wrap around” the edges of the chip on all four of its sides. The socket that houses the PLCC is attached by solder to the circuit board, and the PLCC is held in the socket by friction.
- b. **quad flat pack package:** The QFP package has pins on all four sides, and they extend outward from the package, with a downward-wiring shape. The QFP's pins are much thinner than those on a PLCC, which means that the package can support a larger number of pins; QFPs are available with more than 200 pins.

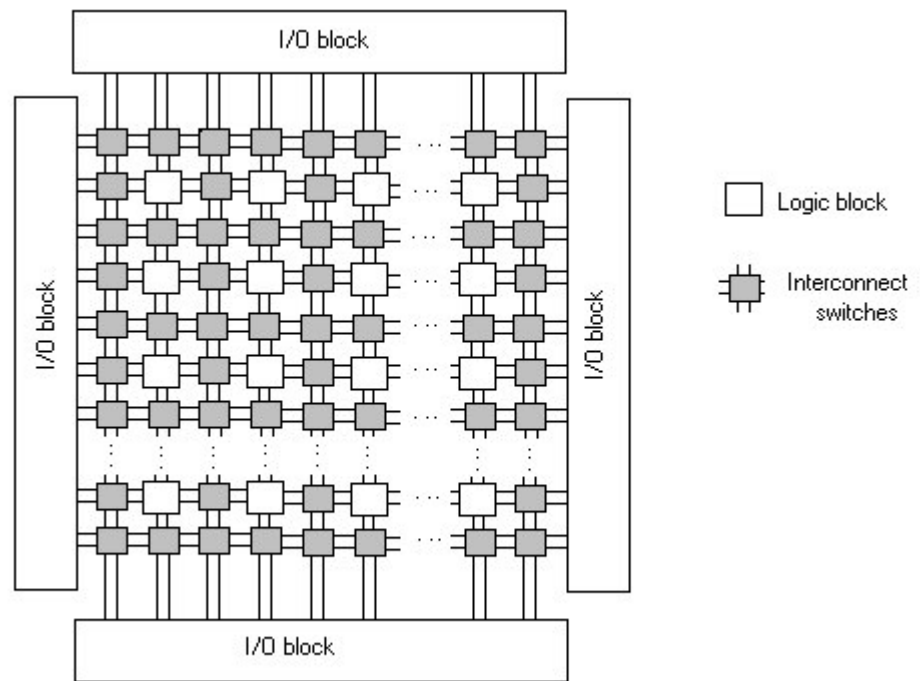
7. Give the structure of MAX 7000 CPLD.



8. What is meant by FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates. FPGAs are quite different from CPLDs because FPGAs do not contain AND or OR planes. Instead, they provide logic blocks for implementation of the required functions.

9. Give the general structure of FPGA.



10. What are the different commercial FPGA products?

Manufacturer	FPGA products	www Locator
Actel	Act 1,2 and 3,MX,SX	www.actel.com
Altera	FLEX6000,8000 and 10k APEX 20k	www.altera.com
Atmel	AT6000, AT40k	www.atmel.com
Lucent	ORCA 1,2 and 3	www.lucent.com
QuickLogic	pASIC 1,2 and 3	www.quicklogic.com
Vantis	VFI	www.vantis.com

Xilinx	XC3000,XC4000,XC5200, Virtex	www.xilinx.com
--------	---------------------------------	--

UNIT 5

VHDL

1) Write the acronym for VHDL?

VHDL is an acronym for **VHSIC** Hardware Description Language (VHSIC is an acronym for Very High Speed Integrated Circuits).

2) What are the different types of modeling VHDL?

- 1) Structural modeling
- 2) Data flow modeling
- 3) behavioral modeling
- 4) Mixed type of modeling

3) What is packages and what is the use of these packages

A package declaration is used to store a set of common declaration such as components types procedures and functions these declaration can then be imported into others design units using a use clause.

4) What is variable class ,give example for variable

An object of variable class can also hold a single value of a given type , However in this case different values can be assigned to a variable at different time.

Ex:variable ss: integer;

5) Name two subprograms and give the difference between these two.

- 1) Function 2) procedure
- Only one output is possible in function..
Many outputs possible using procedure

6) What is subprogram Overloading

If two or more subprogram to be executed in a same name. overloading of subprogram should be performed.

7) write the VHDL coding for a sequential statement (d-flipflop)

```
entity dff is
port(clk,d:in std_logic;
q:out std_logic);
end;
architecture dff of dff is
begin
process(clk,d)
begin
if clk'event and clk='1' then
q<=d;
end process;
end;
```

8) What are the different kinds of The test bench

Stimulus only

Full testbench

Simulator specific

Hybrid testbench

Fast testbench

9) What is Moore FSM

The output of a Moore finite state machine(FSM) depends only on the state and not on its inputs. This type of behaviour can be modeled using a single process with the case statement that switches on the state value.

10) Write the testbench for and gate

```
entity testand2 is
```

```
end entity
```

```
architecture io of testand2 is
```

```
signal a,b,c:std_logic;
```

```
begin
```

```
g1:entity work.and2(ex2) port map(a,b,c)
```

```
a<='0','1' after 100 ns;
```

```
b<='0','1' after 150 ns;
```

```
end;
```